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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/664,094	09/19/2000	Masayuki Mizuno	Q60884	5281

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/664,094	Applicant(s) MIZUNO, MASAYUKI	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment A filed 5/14/2002 has been entered as Paper No. 7. The examiner has considered Amendment A prior to this Office Action. Please be referred to "Response to Arguments" for a reply by the examiner to the Remarks by Applicant filed with Amendment A. In Amendment A all claims (claims 1-9) have been substantially amended. Therefore, said reply only will address those aspects still pertinent to the once amended claims currently outstanding, i.e., newly amended claims 1-9.

Response to Arguments

Applicant points out that one item in the Information Disclosure Statement of Paper No. 5 has not been signed. This is corrected in the present Office Action: please see the corrected Information Disclosure Statement complete with signature on JP-1187512.

With regard to the art rejections under 35 U.S.C. §102(b) of claims 1-7 as anticipated by Toyoda et al (JP405166965A) and the rejections under 35 U.S.C. §103(a) as unpatentable over Toyoda et al (JPO405166965A), Applicant's arguments are found to be moot. Applicant asserts that the feature in Applicant's invention that "holes or slits are formed in the signal lines or ground plate so as to increase the characteristic impedance between adjacent signal lines or between one signal line and the ground plate" is neither disclosed nor suggested by the cited reference. However,

the examiner specifically refers to "signal transmission line (cf. "Constitution", second sentence) of a microstrip structure (cf. "Abstract", first sentence) composed of an insulating board or ground plate 44 and signal line 46 controlled in specific impedance by holes formed in said signal line (cf. through-holes in signal line as evidenced in Figures 1 and 3, numeral 48), while Applicant does not specifically address in what way or manner this characterization of the teaching of Toyoda et al is incorrect. On the basis of the examiner's characterization, obtained straightforwardly from the cited reference, it is clear that holes or slits are indeed formed in the signal lines or ground plate so as to increase the characteristic impedance between the adjacent signal lines or between one signal line and the ground plate. Therefore, the rejections are herewith essentially repeated to the extent allowed by the amendment of the claim language.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 102(b) as being anticipated by Toyoda et al (JP405166965A). With reference to "Abstract: Purpose and Constitution": Toyoda et al teach a package structure with semiconductor chip 42, hence a semiconductor integrated circuit comprising a signal transmission line (cf. "Constitution", second sentence) of a micro-strip structure (cf. "Abstract, first sentence) composed of an

insulating board or ground plate 44 and a signal line 46 controlled in specific impedance by holes formed in said signal line (cf. through-holes in signal line as evidenced in Figs. 1 and 3, numeral 48). In conclusion, Toyoda et al anticipate claim 1.

3. ***Claim 2*** *is rejected* under 35 U.S.C. 102(b) as being anticipated by Toyoda et al (JP405166965A). With reference to "Abstract: Purpose and Constitution": Toyoda et al teach a package structure with semiconductor chip 42, hence a semiconductor integrated circuit comprising a signal transmission line (cf. "Abstract: Constitution", second sentence) of a micro-strip structure (cf. "Abstract, first sentence) composed of an insulating board or ground plate 44 and a signal line controlled in specific impedance by holes formed in said signal line (cf. through-holes 56 and 58 in ground plate as evidenced in Figs. 1 and 3). In conclusion, Toyoda et al anticipate claim 2.

4. ***Claims 3-4*** *are rejected* under 35 U.S.C. 102(b) as being anticipated by Toyoda et al (JP405166965A).

With regard to claim 3: Toyoda et al teach a package structure (cf. "Abstract: Purpose", first sentence) comprising a semiconductor microchip 42 (cf. "Abstract: Constitution", first sentence) comprising a signal transmission line 46 (cf. Abstract: Constitution", second sentence) and a ground plate or insulating board 44 (cf. "Abstract: Constitution", first sentence) according to claim 2, wherein the size of the aforementioned at least one hole or through-holes 56 and 58 (cf. "Abstract: Purpose", final sentence, see also Figs. 1 and 3) formed in said ground plate 44 is determined such that the AC coupling between the signal line 46 and another signal line or rear-side

signal line 50 (cf. "Abstract: Constitution", second sentence) disposed close to said signal line 46 but on the opposite side of said ground plate 44 is decreased and the characteristic impedance of said signal transmission line 46 is increased (cf. "Abstract: Purpose", final sentence). That in fact the AC coupling is decreased follows from the well-known relationship in physics between the AC coupling and the impedance through capacitance, and as such is an inherent aspect, given the stated purpose and constitution by Toyoda et al. Therefore, Toyoda et al anticipate claim 3.

With regard to claim 4: because it is the very purpose of Toyoda et al to control said impedance by providing said through-holes the further limitation of claim 4 is an inherent aspect of the constitution given the trivial relationships between conductor surface area, capacitance, frequency, impedance and AC coupling.

5. ***Claims 5-7*** *are rejected* under 35 U.S.C. 102(b) as being anticipated by Toyoda et al (JP405166965A). Toyoda et al teach a semiconductor integrated circuit (cf. "Abstract: Purpose", first sentence, and "Abstract: Constitution", first sentence, in particular reference to package and semiconductor chip 42) comprising a signal transmission line 46 of a micro-strip structure (cf. "Abstract: Constitution", second sentence) composed of a signal line or surface-side signal line 46 (cf. "Abstract: Purpose", and "Abstract: Constitution", first sentence) and ground plate or insulating board 44 (cf. Abstract: Constitution", second sentence) wherein at least one hole (through-hole 56 and 58, cf. "Abstract: Constitution", first sentence) is formed in both of said surface-side line 46 and rear-side signal line 50 (cf. "Abstract: Constitution", second sentence) throughout (cf. "Abstract: Purpose") ground plate 44. See also Figs. 1 and 3.

With regard to claim 6: Toyoda et al teach a package structure (cf. "Abstract: Purpose", first sentence) comprising a semiconductor microchip 42 (cf. "Abstract: Constitution", first sentence) comprising a signal transmission line 46 (cf. Abstract: Constitution", second sentence) and a ground plate or insulating board 44 (cf. "Abstract: Constitution", first sentence) according to claim 5, wherein the size of the aforementioned at least one hole or through-holes 56 and 58 (cf. "Abstract: Purpose", final sentence, see also Figs. 1 and 3) formed in said ground plate 44 is determined such that the AC coupling between the signal line 46 and another signal line or rear-side signal line 50 (cf. "Abstract: Constitution", second sentence) disposed close to said signal line 46 but on the opposite side of said ground plate 44 is decreased and the characteristic impedance of said signal transmission line 46 is increased (cf. "Abstract: Purpose", final sentence). That in fact the AC coupling is decreased follows from the well-known relationship in physics between the AC coupling and the impedance through capacitance, and as such is an inherent aspect, given the stated purpose and constitution by Toyoda et al. Therefore, Toyoda et al anticipate claim 6.

With regard to claim 7: because it is the very purpose of Toyoda et al to control said impedance by providing said through-holes the further limitation of claim 7 is an inherent aspect of the constitution given the trivial relationships between conductor surface area, capacitance, frequency, impedance and AC coupling.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. ***Claims 8 – 9*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al (JP405166965A).

With regard to claim 8: as detailed above, Toyoda et al anticipate both claims 1 and 2, on which claims 9 and 8 depend, respectively. Toyoda et al do not specifically teach to implement the control of the specific impedance of the transmission lines by varying the *size* or *shape* of the aforementioned through-holes. However, Toyoda et al do point out that the through-holes are introduced so that the specific impedance of the transmission lines can be "controlled". Because there is more than one transmission line in Toyoda et al (surface-side and rear-side transmission lines 46 and 50) it is an obvious step to modify the impedance of one transmission line more than the other in accordance with design requirements, while it is equally obvious that a bigger hole means a greater modification of said impedance. Applicants are furthermore reminded of the circumstance that a change in size is generally recognized as being within the level of ordinary skills in the art (In re Rose, 105 USPQ 237 (CCPA 1955)).

With regard to claim 9: because a slit hole can be constituted by a plurality of connected circular holes while substantially circular holes have been disclosed by

Toyoda et al, the question with regard to claim 9 is whether the number of holes has patentable weight. Considering the substantial equivalence between the method of controlling impedance by modifying the size of a single hole and the method of controlling impedance by modifying the number of holes, the remarks above with reference to In re Rose, 105 USPQ 237 (CCPA 1955) also apply to claim 9.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
July 18, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800